Low Noise, high linearity, wide bandwidth Amplifier using a 0.35µm SiGe BiCMOS for WLAN applications.

J.Sadowy[1,2], I.Telliez[2], J.Graffeuil[1,3], E.Tournier[1,3], L. Escotte[1,3] and R. Plana[1,3].

1) LAAS CNRS 7, Av du Colonel Roche 31077 Toulouse
2) STMicroelectronics 850, rue Jean Monnet 38926 Crolles Cedex
3) Université P. Sabatier, Toulouse, France

ABSTRACT — In this paper, we present the design of an integrated low noise amplifier (LNA) for WLAN applications in the 6 GHz range using a low complexity SiGe BiCMOS technology. The SiGe HBTs used in the design feature a typical cut-off frequency "Ft" of 45 GHz and a typical maximum oscillation frequency "Fmax" of 60 GHz.

The LNA exhibits a 17 dB power gain with a 1.4 GHz bandwidth and a noise figure lower than 2.5 dB. The 1 dB compression point is -18 dBm and the third order intercept point referred to the input is -7 dBm. We have furthermore observed a good accuracy between simulations and measurements. Finally, we have defined a new figure of merit involving the noise measure and the DC power consumption that shows that our design features a performance at the state of the art.

I. INTRODUCTION

The multiplication of wireless telecommunication systems and the increase of the number of customers translate into very strict requirements concerning the performance of the microwave modules. They have to feature a low noise figure and a high linearity due to the overcrowding spectrum. They have also to exhibit the best low power consumption as possible in order to meet with the customer requirements and finally they have to be cheaper and cheaper. Among the electronic modules which are playing a key role in the front-end performance, we must consider the low noise amplification module.

These last years have seen the emergence of a new contender for the microwave applications: the SiGe HBT. This type of component features maximum operating frequencies beyond 50 GHz, which makes possible to use it up to 20 GHz and more. It further exhibits excellent properties in term of noise (both in the high frequency range for low noise amplifier and in the low frequency range for low phase noise oscillator). Moreover, SiGe BiCMOS technology is a silicon-based technology that takes advantage of the maturity of silicon processing techniques and results into low cost components. If the situation concerning the active device seems to be clear, the problem of the passive elements on silicon is still pending despite the tremendous efforts that have been made for many years to overcome the drawbacks inherent to the silicon substrate.

With this end in view, we address the design of a 5 GHz to 6 GHz low noise amplifier for WLAN applications such as HIPERLAN. The work is based on a low complexity SiGe BiCMOS process of ST Microelectronics. The emitter width is 0.35 µm. For this work, we use the low voltage version exhibiting the higher Fmax value in order to get a low value of the noise figure. Such a device exhibits a current gain of about 90 and Ft and Fmax values of 45 GHz and 60 GHz respectively. The electrical behavior of the device is described through a modified "Gummel Poon" non linear model which has been validated up to 20 GHz. Concerning the passive elements, the technology features five aluminum metal levels, which makes possible the realization of a large range of capacitances and inductors featuring Q's in excess of 10.

The first section addresses the LNA design and the second section presents the experimental results. Section III compares the performances of our circuit with recent published data. Finally, conclusions will be outlined in the last section of this paper.

II. LNA DESIGN

The design of a LNA in the microwave range usually requires two stages. The total noise figure is given by the following expression [1]:

$$NF = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 * G_2} + \dots \quad (1)$$

Where NF_i and G_i represent the noise figure and the gain of the ith stage respectively.

Figure 1 shows the amplifier circuit. Cascode topology [2,3] was retained for various reasons. First, the cascode amplifier has the advantage of providing gain, to be low noise and it is a very stable circuit featuring a very large isolation and a large frequency bandwidth. Transistor T1 provides the gain of the amplifier whereas the transistor T2 provides the reverse isolation, by

217

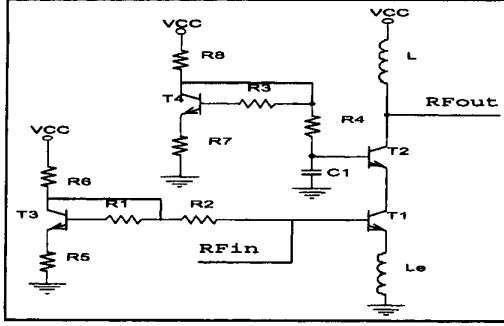removing the Miller effect of the base-collector capacitance of transistor T1.

Fig. 1: simplified schematic of the low noise amplifier.

Fig. 2: Layout of the low noise amplifier

One of the key point of the LNA is related to the fact that usually the power input matching impedance and the input noise matching impedance are very different making very difficult to have simultaneously a high gain and a low noise figure. A very well known technique is used to overcome this problem. First, the transistor size and bias are adjusted in order to have an appropriate value for the optimum noise impedance. Then a degeneration inductance "Le" [4,5], placed between the emitter of T1 and the ground is used to provide both the power and noise matching. The value of this inductance is given by the following equation [4,5]:

$$Le \approx \frac{50}{2.\pi.F_t} \quad (2)$$

From the transition frequency of the SiGe HBT used in this work and using equation (2), we found an inductor value of about 0,15 nH. An appropriate inductor layout featuring this value has been obtained through a dedicated electromagnetic simulation. It must be emphasized that the design of such an accurate, high Q, integrated small value inductor needs to be specifically addressed through electrical and electromagnetic simulations because it has a major impact on the circuit performance. The quality factor of the inductor is in the 10 range at 6 GHz and its resonance frequency in the 40 GHz range. More details on the design will be outlined at the conference.

The design of the LNA has been done using a commercial software. The LNA features a DC bias voltage of 3.3 V and the total power consumption is 13 mW. The circuit has been processed by ST Microelectronics. The layout is presented in figure 2. The chip size is 1.4 mm^2. Special attention has been paid to minimize the parasitic and to optimize the silicon surface.
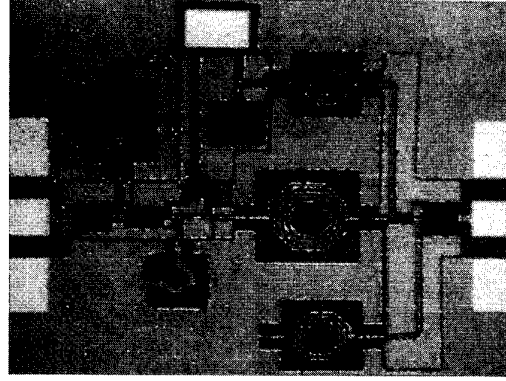
Next section deals with the results that have been obtained.

III. RESULTS

The circuit has been on wafer measured using appropriate coplanar probes in order to characterize a circuit featuring an aluminum metallization. The linear and nonlinear measurements have been performed thank to a network analyzer "SCORPIO" supplied by ANRITSU. Figure 3 shows the measured gain and the measured noise figure from 4 GHz to 7 GHz. Measurements indicate a maximum gain value of about 17 dB. We obtain a minimum noise figure value lower than 2.6dB, which is very close to the state of the art for a BiCMOS SiGe 0.35 μm, aluminum metal technology.
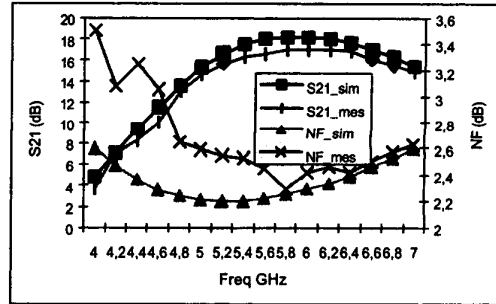

Fig. 3: Gain (|S21|) and the noise figure (NF) vs. frequency

Finally, concerning the frequency bandwidth, measurements show a 1.4 GHz bandwidth between 5.2 GHz and 6.6GHz whereas 1.5 GHz was expected from electrical simulations. The difference is attributed to a shift in the output impedance matching. This has to be clarified, we will present more details at the conference.

218

The isolation performance is in the −40 dB range all over the bandwidth.

We have investigated the non-linear behavior of the amplifier through 1 dB compression point and third order intermodulation characterizations referred to as IM3. Figure 4 presents the non-linear measurements carried out on the low noise amplifier. The measured 1 dB compression is in the −18 dBm range. Concerning the IM3 investigations, they have been carried out by injecting two tones RF signals separated by 10 kHz. We can observe, in figure 4, that IM3 data show a slope of 3 as predicted by the theory. The measured IIP3 is close to −7 dBm, which shows that the linearity performance of the circuit is good. We also have to outline that the measurements compare very well with the simulation validating the non-linear model and the design method (i.e. a special attention has been paid to take into account the parasitics).
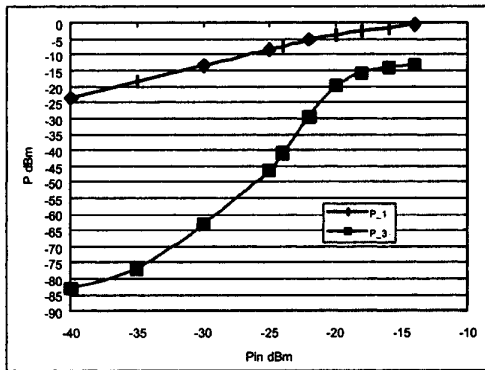

Fig. 4: Characterization of the LNA in the non-linear regime.

Finally, we will discuss our data from comparisons with same others picked up in the literature

IV. COMPAREASON AND DISCUSSION

First of all we show in table 1 a comparison between our results and one of the best-reported results [3] in the same frequency range.

	Cascode (This work)	2 stages [3]
Technology	SiGe (ST)	SiGe (Temic)
Supply voltage	3.3V	4.5V
Power	13mW	33.7mW
Gain max	17dB	23dB
Bandwidth	1.4 GHz	Very narrow
NF	2.3	1.6dB
P_{1dBin}	-18dBm	-22dBm
IIP3	-7dBm	-13dBm

Table 1 : comparative study of the electrical behavior of two SiGe LNA.

This comparison indicates that our circuit features a lower supply voltage, a lower power consumption, a larger bandwidth and greater linearity performances than the other circuit, which exhibits better noise performance.

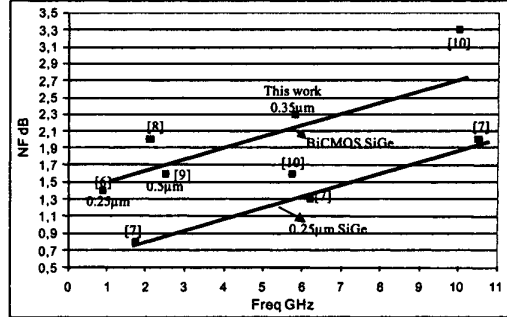Figure 5 compares the state of the art [6-10] with our results about the noise figure NF.

Fig. 5: Evolution of Noise Figure NF vs. frequency.

Our work is close to the state of the art with a BiCMOS SiGe 0.35μm technology. As expected, the best performances are obtained for a pure 0.25μm SiGe technology.

The second figure of merit, we have inspected deals with the ratio between the power gain and the DC power consumption referred to as Fm (dB/mW). The results are displayed in figure 6. We can observe that most of the already published results turn out to a figure of merit lower than 1 dB/mW whereas our design features a value of 1.3 dB/mW.
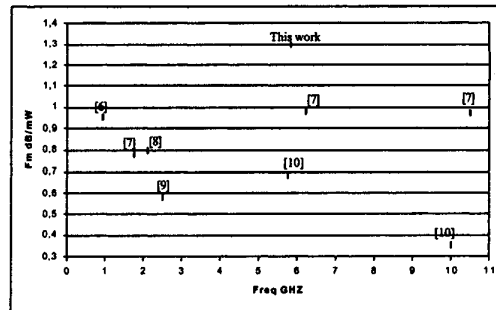

Fig. 6: Evolution of Fm vs. frequency.

An usual way to evaluate the potentialities of a LNA is to calculate a quantity called *Noise Measure* (M), which is defined by the following expression:

$$M = \frac{NF-1}{1-\frac{1}{G}} \quad (3)$$

where NF corresponds to the noise figure and G represents the power gain of the circuit. M is actually a

trade off between a low value of the noise figure and high power gain value. Nevertheless, this figure of merit does not take into account the DC power consumption. Therefore we propose an extended figure of merit, which is obtained by multiplying the factor M by the DC power consumption (M*P) and that has to be as low as possible.

Figure 7 represents the evolution of this new figure of merit versus frequency for a set of recently published low noise amplifiers in the RF frequency band.
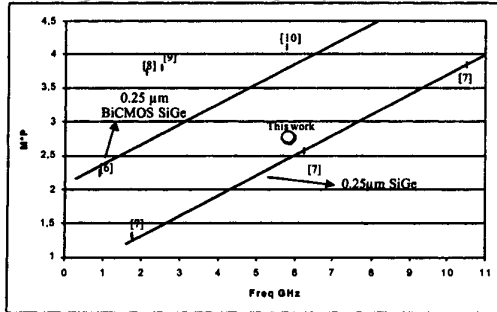

Fig. 7: M*Power DC vs. frequency.

From equation 3, it is understood that the figure of merit M has to be as low as possible. The new figure of merit feature the same properties. From the results plotted in figure 7, we can see that we have two distinct regions. One region, mostly represented by different published LNA's based on a 0.25 µm SiGe technology, featuring the lowest figure of merit . The second one features an highest figure of merit and is related to other published LNA's realized through BiCMOS SiGe technology featuring emitter width ranging from 0.25 µm to 0.8 µm. We can observe that our circuit exhibits a figure of merit near the one of a 0.25µm technology (usually featuring Cu metal) although it has been processed, in our case, with a 0.35µm aluminum metal one. We therefore believe that we have a provision for further improvements and this point will be outlined at the conference.

IV CONCLUSION

This paper reports on the design and characterization of a low noise amplifier for WLAN applications in the 6 GHz range. The LNA features a very wide bandwidth, high gain and a noise figure in the 2.3 dB range. This result is at the state of the art for a BiCMOS SiGe technology featuring 0.35 µm emitter width. We have measured a maximum power gain of 17dB, a 1dB compression in the -18dBm range and an IIP3 in the -7dBm range, which is a good result specially if the low voltage supply (3.3 V) and the low power consumption (13 mW) are considered.

Finally, we have defined a new figure of merit involving the noise figure, the gain and the DC power consumption.

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